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IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A computerized method of creating a layout for a circuit design performed by a computer aided design tool, the method comprising:

receiving a circuit design;

receiving at least one layout rule based on a reliability verification constraint ~~arising from self heat~~; ~~and~~

generating a circuit layout for the circuit design through computer automated operations;

performing an analysis of the circuit layout to determine whether the circuit layout satisfies the at least one layout rule;

if the analysis indicates that the circuit layout does not satisfy a rule of the at least one layout rule, automatically rearranging portions of the circuit layout, to produce a revised circuit layout; and

repeating the performing and automatically rearranging of the revised circuit layout until ~~wherein the~~ the revised circuit layout generated satisfies the at least one layout rule based on the reliability verification constraint received for the circuit design.

2. (Previously Presented) The computerized method of claim 1, further comprising receiving at least one layout rule based on a reliability verification constraint arising from electromigration.

3. (Canceled)

4. (Original) The computerized method of claim 1, wherein the at least one layout rule defines a maximum current for a given wire width.

5. (Original) The computerized method of claim 1, wherein the circuit design is a microprocessor circuit design.

6. (Currently Amended) The computerized method of claim 1, wherein the circuit layout is a two-dimensional layout comprising a plurality of overlapping rows.

7. (Currently Amended) A computer automated placement method performed by a computer aided design tool, the method comprising:

placing a plurality of components of an integrated circuit design in a circuit layout for the integrated circuit design;

~~analyzing~~ performing an analysis of the circuit layout ~~for~~ based on reliability verification considerations ~~arising from self heat~~;

if the analysis indicates that the circuit layout does not adequately address the reliability verification considerations, automatically rearranging the plurality of components to improve the reliability verification considerations; and

repeating the ~~analyzing~~ performing and the rearranging to further improve the reliability verification considerations.

8. (Currently Amended) The computer automated placement method of claim 7, wherein ~~analyzing the layout for reliability verification considerations~~ performing the analysis further includes analyzing for electromigration considerations.

9. (Canceled)

10. (Original) The computer automated placement method of claim 7, further comprising analyzing the layout for other considerations selected from the group consisting of: layout density constraints, aspect ratio constraints, and routing complexity constraints.

11. (Original) The computer automated placement method of claim 7, wherein placing the plurality of components is done in a two-dimensional manner with a plurality of overlapping rows.

12. (Currently Amended) The computer automated placement method of claim 7, wherein ~~analyzing the layout~~ performing the analysis is performed by calculating an overall unidirectional current density for the layout.

13. (Currently Amended) A computerized method of placing a plurality of components of an integrated circuit in a layout, the method comprising:

assigning each one of a plurality of components of an integrated circuit to one of a plurality of clusters;

generating a layout for each one of the plurality of clusters;

placing each one of the plurality of clusters in a layout for the integrated circuit wherein the placing is performed in a two-dimensional manner with a plurality of overlapping rows;

~~analyzing~~ performing an analysis of the layout for the integrated circuit using a cost function having a reliability verification factor; and

automatically rearranging the layout for the integrated circuit by automatically rearranging the plurality of clusters; and

repeating the analyzing and the rearranging until the cost function is minimized.

14. (Original) The computerized method of claim 13, wherein the reliability verification factor represents the effects of electromigration and self heat.

15. (Original) The computerized method of claim 13, wherein a width of each one of the plurality of overlapping rows is a multiple of a smallest one of the plurality of clusters.

16. (Original) The computerized method of claim 14, wherein assigning each one of the components is performed based on a lumped gate ordering style.

17. (Original) The computerized method of claim 14, wherein assigning each one of the components is performed based on a distributed gate ordering style.

18. (Original) The computerized method of claim 14, further comprising adjusting one or more of the plurality of components in one of the clusters to comply with a size constraint.

19. (Original) The computerized method of claim 18, wherein the adjusting is performed using device-based legging.

20. (Original) The computerized method of claim 18, wherein the adjusting is performed using stack-based legging.

21. (Original) The computerized method of claim 18, wherein the adjusting is performed using differential legging.

22. (Currently Amended) An article comprising:

a computer-readable medium including instructions that when executed cause a computer to:

receive a circuit design;

receive at least one layout rule based on a reliability verification constraint ~~arising from self heat; and~~

generate a circuit layout for the circuit design through computer automated operations;

perform an analysis of the circuit layout to determine whether the circuit layout satisfies the at least one layout rule;

if the analysis indicates that the circuit layout does not satisfy a rule of the at least one layout rule, automatically rearrange portions of the circuit layout, to produce a revised circuit layout; and

repeat the performing and automatically rearranging of the revised circuit layout until ~~wherein the~~ the revised circuit layout generated satisfies the at least one layout rule based on the reliability verification constraint received for the circuit design.

23. (Original) The article of claim 22, wherein the reliability verification constraint arises from electromigration.

24. (Canceled)

25. (Original) The article of claim 22, wherein the layout is generated in a two dimensional manner having a plurality of overlapping rows.

26. (Currently Amended) An article comprising:

a computer-readable medium including instructions that when executed cause a computer to:

place a plurality of components of an integrated circuit design in a two-dimensional circuit layout for the integrated circuit design;

~~analyze~~ perform an analysis of the circuit layout ~~for~~ based on reliability verification considerations ~~arising from self heat~~; ~~and~~

if the analysis indicates that the circuit layout does not adequately address the reliability verification considerations, automatically rearrange the plurality of components to improve the reliability verification considerations based on the analysis of the circuit layout; and

repeat the performing and the rearranging to further improve the reliability verification considerations.

27. (Original) The article of claim 26, wherein the reliability verification consideration arises from electromigration.

28. (Canceled)

29. (Currently Amended) A computer-readable medium having computer-executable modules comprising:

a cell library to maintain a plurality of logic gates and a plurality of layout rules;

a schematic design tool to create a schematic of an integrated circuit using the plurality of gates maintained by the cell library;

a net list tool to create a net list representation of the schematic; and

a placement tool to generate a revised circuit layout of the integrated circuit from the net list representation wherein the placement tool performs a reliability verification of the layout ~~for self heat considerations~~, the reliability verification including

receiving a circuit design,

receiving at least one layout rule based on a reliability verification constraint,

generating a circuit layout for the circuit design through computer automated operations;

performing an analysis of the circuit layout to determine whether the circuit layout satisfies the at least one layout rule,

if the analysis indicates that the circuit layout does not satisfy a rule of the at least one layout rule, automatically rearranging portions of the circuit layout, to produce the revised circuit layout, and

repeating the performing and automatically rearranging of the revised circuit layout until the revised circuit layout generated satisfies the at least one layout rule based on the reliability verification constraint received for the circuit design.

30. (Original) The computer-readable medium of claim 29 further comprising a routing tool to route wires between the plurality of logic gates in the layout.

31. (Currently Amended) A computerized system comprising:

a computer-readable medium;

a processor; and

a computer-aided design program stored on the computer-readable medium and executable by the processor, the computer-aided design program comprising a placement module to generate a layout of an integrated circuit wherein the placement module performs a reliability verification of the layout for at least one reliability verification constraint, the reliability verification including

receiving a circuit design,

receiving at least one layout rule based on a reliability verification constraint selected from a group of constraints that includes self heat and electromigration considerations,

generating a circuit layout for the circuit design through computer automated operations;

performing an analysis of the circuit layout to determine whether the circuit layout satisfies the at least one layout rule,

if the analysis indicates that the circuit layout does not satisfy a rule of the at least one layout rule, automatically rearranging portions of the circuit layout, to produce the revised circuit layout, and

repeating the performing and automatically rearranging of the revised circuit layout until the revised circuit layout generated satisfies the at least one layout rule based on the reliability verification constraint received for the circuit design.

32. (New) The computerized method of claim 1, wherein the at least one layout rule based on the reliability verification constraint includes at least one constraint selected from a group of constraints consisting of electromigration, self heat, and a combination thereof.

33. (New) The computerized method of claim 1, wherein automatically rearranging portions of the layout comprises:

automatically rearranging the relative locations of one or more transistors.

34. (New) The computerized method of claim 1, further comprising:

assigning each transistor of the circuit design to a cluster, to produce multiple clusters;

generating a cluster layout for each cluster, to produce multiple cluster layouts; and

wherein generating the layout includes arranging the multiple layout clusters.

35. (New) The computerized method of claim 33, wherein automatically rearranging portions of the layout comprises:

automatically rearranging the multiple cluster layouts.

36. (New) The computerized method of claim 33, wherein assigning each transistor to a cluster comprises:

initially assigning each transistor to a preliminary cluster, resulting in multiple preliminary clusters;

merging the preliminary clusters to produce the multiple clusters; and

adjusting the multiple clusters.

37. (New) The computerized method of claim 33, wherein generating a cluster layout comprises:

building diffusion graphs for portions of the multiple clusters;

finding paths in the diffusion graphs; and

generating the multiple cluster layouts based on the paths.

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38. (New) The computerized method of claim 1, wherein the at least one layout rule is based on a reliability verification constraint for interconnections between transistors of the circuit.

39. (New) The computerized method of claim 1, wherein each of the portions of the circuit layout includes at least one transistor.